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NASA TECH BRIEF

Marshall Space Flight Center

Techniques for Improving Reliability of Computers

The problem:

Future computer requirements indicate the need for an increase in reliability by a factor of at least 10. These improvements cannot result in an undue increase of power dissipation, processing time, or the time required for system recovery from a malfunction.

The solution:

Modular design techniques result in the enhancement of computer reliability by improving methods of error detection, diagnosis, and recovery.

How it's done:

A theoretical computer, MARCS (Modular Architecture for Reliable Computer Systems), was designed with the following objectives:

A modular system organization for easier error detection, diagnosis, self-repair, and a significantly lower level of redundancy.

Error monitoring and detection by hardware at the module level.

Distinction between transient and permanent failures and catastrophic and non-catastrophic failures.

System-aided recovery and reconfiguration for optimizing system effectiveness after error detection.

Program detection and isolation of aberrant hardware.

The study deals with a postulated and modeled technology indigenous to 1975-1980. Correction schemes fundamental to a modular structure are considered which include Triple Modular Redundancy, Quadding and Sparing. The organization factor of reliable machine design is characterized as logic-based through the architectural structure of the machine and the fashion in which hardware error detection and correction is incorporated into the structure by the design techniques. The aspect of algorithms used in interactive design by the basic processes of recovery and diagnosis are defined and examined for error detection hardware and system organization.

Several important developments have arisen from the MARCS study. They include:

1) The use of Morphic Boolean Functions.
2) The new form of Boolean Difference.
3) Diagnosis procedures prescribable by the RCVY (Recovery - an interactive programming language) Program.
4) Self-testable implementations of Hamming SEC/DED (Single Error Correcting/Double Error Detecting) encoding and decoding circuitry.
5) A basic design of the Configuration assignment unit module.
6) Input/Output Processor specification and design using error detecting shift register control units.

Note:

Requests for further information may be directed to:

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Patent status:

Inquiries concerning rights for the commercial use of this invention should be addressed to:

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